AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Listing of claims.

1. (Original) A semiconductor device, comprising:

an insulating resin layer; and

a semiconductor chip mounted on said insulating layer;

wherein said insulating resin layer includes a patterned interconnect line embedded therein, and

wherein said insulating resin layer has a relative dielectric constant within a range from 1.0 to 3.7, and a dielectric loss tangent within a range from 0.0001 to 0.02.

2. (Original) The semiconductor device according to claim 1, wherein water absorption of said insulating resin layer is equal to or less than 0.1 %.

3. (Original) The semiconductor device according to claim 1, wherein said insulating resin layer includes a patterned interconnect line having a multi-layer structure embedded therein.

4. (Original) The semiconductor device according to claim 1, wherein said insulating resin layer contains liquid crystal polymer, epoxy resin or BT resin.

5. (Original) The semiconductor device according to claim 1, wherein surface roughness Ra of said patterned interconnect line is equal to or less than 1 μm.

6. (Original) The semiconductor device according to claim 1, wherein said semiconductor chip is flip-chip mounted on said insulating layer.

7. (Currently Amended) A semiconductor device, comprising:

an insulating resin layer; and

a semiconductor chip mounted on said insulating layer;

wherein said insulating resin layer includes a patterned interconnect line embedded therein, and

wherein the coefficient of thermal expansion of said insulating resin layer is within a range from -5 to 5ppm/degree centigrade ~~(excluding zero)~~.

8. (Original) A method for manufacturing a semiconductor device, comprising:

providing a semiconductor device-forming region on a surface of a substrate;

forming a layer structure in said semiconductor device-forming region on said substrate, said layer structure including an insulating resin layer and a patterned interconnect line being embedded in said insulating resin layer;

mounting a semiconductor chip on said layer structure, respectively;

molding said semiconductor chip with an insulating material in said semiconductor device-forming region;

removing said substrate;

exposing at least a part of said patterned interconnect line; and

dicing said insulating resin outside said semiconductor device-forming region and separating thereof into a module-forming unit to form a semiconductor device,

wherein a material of said insulating resin layer is a resin having a relative dielectric constant within a range from 1.0 to 3.7, and a dielectric loss tangent within a range from 0.0001 to 0.02.

9. (Original) The method according to claim 8, wherein a material of said insulating resin layer is a resin having a water absorption of equal to or less than 0.1 %.

10. (Original) The method according to claim 8, wherein said forming the layer structure includes embedding said patterned interconnect line having a multi-layer structure in said insulating resin layer.

11. (Original) The method according to claim 8, wherein a material of said insulating resin layer is a resin containing liquid crystal polymer, epoxy resin or BT resin.

12. (Original) The method according to claim 8, wherein said forming the layer structure includes:

forming said insulating resin layer over said substrate;

providing a connecting hole in said insulating resin layer;

forming a metal film to fill said connecting hole; and

selectively etching said metal film to form said patterned interconnect line.

13. (Original) The method according to claim 12, wherein said substrate is an electrical conductive substrate, and wherein at least a part of said metal film is formed via an electrolytic plating method, in which said electrical conductive substrate is utilized as an electrode thereof.

14. (Original) The method according to claim 12, further comprising:

conducting a surface processing after forming the metal film to achieve a surface roughness Ra of said metal film equal to or less than 1 μm.

15. (Original) The method according to claim 8, wherein said mounting the semiconductor chip on the layer structure includes flip-chip mounting said semiconductor chip on said layer structure.

16. (Currently Amended) A method for manufacturing a semiconductor device, comprising:

providing a semiconductor device-forming region on a surface of a substrate;

forming a layer structure in said semiconductor device-forming region on said substrate, said layer structure including an insulating resin layer and a patterned interconnect line being embedded in said insulating resin layer;

mounting a semiconductor chip on said layer structure, respectively;

molding said semiconductor chip with an insulating material in said semiconductor

device-forming region;

removing said substrate;

exposing at least a part of said patterned interconnect line; and

dicing said insulating resin outside said semiconductor device-forming region and separating thereof into a module-forming unit to form a semiconductor device,

wherein the coefficient of thermal expansion of said insulating resin layer is within a range from -5 to 5ppm/degree centigrade ~~(excluding zero)~~.

17. (Original) A thin plate interconnect line member having a semiconductor chip-mounting surface and an interconnect line substrate-coupling surface opposite to said chip-mounting surface, comprising:

an insulating resin layer; and

a patterned interconnect line being embedded within said insulating resin layer,

wherein at least a part of said patterned interconnect line is exposed on said interconnect line substrate-coupling surface, and

wherein said insulating resin layer has a relative dielectric constant within a range from 1.0 to 3.7, and a dielectric loss tangent within a range from 0.0001 to 0.02.

18. (Original) The thin plate interconnect line member according to claim 17, wherein water absorption of said insulating resin layer is equal to or less than 0.1 %.

19. (Original) The thin plate interconnect line member according to claim 17, wherein a patterned interconnect line having a multi-layer structure is embedded in said insulating resin layer.

20. (Original) The thin plate interconnect line member according to claim 17, wherein said insulating resin layer contains liquid crystal polymer, epoxy resin or BT resin.

21. (Original) The thin plate interconnect line member according to claim 17, wherein the surface roughness Ra of said patterned interconnect line is equal to or less than 1 μm.

22. (Currently Amended) A thin plate interconnect line member having a semiconductor chip-mounting surface and an interconnect line substrate-coupling surface opposite to said chip-mounting surface, comprising:

an insulating resin layer; and

a patterned interconnect line being embedded within said insulating resin layer,

wherein at least a part of said patterned interconnect line is exposed on said interconnect line substrate-coupling surface, and

wherein the coefficient of thermal expansion of said insulating resin layer is within a range from -5 to 5ppm/degree centigrade ~~(excluding zero)~~.